SIDDHARTH INSTITUTE OF ENGINEERING AND TECHNOLOGY, KORAPUT

DEPARTMENT OF ELECTRICAL ENGINEERING

LESSON PLAN

Name of the Course : TH-1 : DIGITAL ELECTRONICS AND MICROPROCESSOR			
Name of the Faculty: Er. GIRISHABALA GAMANGA			
Semester from date : 01.07.2026 TO 05.11.2026			
Course Code :	EEPC301	Semester :	5th
Total Periods:	45 Periods	Examination :	3Hrs
Theory Periods :	45 Hrs.	Progressive Assessment :	30
Lecture :	3Hrs/week	End Term Exam :	70
Credit :	3	Total Marks :	100

VISION:

To create competent and industry ready Electrical Diploma Engineers with professional and social values to meet future challenges.

MISSION:

- To prepare diploma holders through "qualitative competency-based education system" to compete with national requirement along with core values.
- To produce dynamic Electrical Engineers to serve the society and industry.
- To develop leadership qualities, communication skills, critical thinking and attitude for lifelong learning.

PROGRAM EDUCATIONAL OBJECTIVES:

PEO1	Applying technical knowledge and skills learned in the field of Electrical Engineering to excel in professional and/or higher education.
PEO2	To provide students an excellent academic environment and make them aware the needs of Society and Industry to become a successful Professional/Entrepreneur.
PEO3	To engage in lifelong learning, career enhancement to adopt to emergingtechnologies.

COURSE OUTCOME:

CO1	Apply digital fundamentals, Boolean algebra and its applications in simple digital system
CO2	Comprehend combinational logic circuits
CO3	Illustrate analysis and design procedures for synchronous and asynchronous sequential circuits.
CO4	Explain the various semiconductor memories and related technology.
CO5	Explain the architecture of microprocessor 8085.

TOPIC WISE DISTRIBUTION OF PERIODS

Unit No.	Topics	Periods
I	Digital Fundamentals	08
II	Combinational & Synchronous Sequential Circuits	09
III	Asynchronous Sequential Circuits and Memory devices	09
IV	8085 Processor	09
V	Programming Processor	10

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Week	Day	Theory Topic	Corresponding CO
1st	WEDNESDAY	Number Systems – Decimal, Binary, Octal, Hexadecimal, 1's and 2's complements	CO1
	THURSDAY	Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes	CO1
	FRIDAY	Boolean theorems	CO1
2nd	WEDNESDAY	Logic gates and truth tables	CO1
	THURSDAY	Universal gates, Sum of products and product of sums	CO1
	FRIDAY	Minterms and Maxterms	CO1
3rd	WEDNESDAY	Karnaugh map Minimization	CO1
	THURSDAY	QuineMcCluskey method of minimization	CO1
	FRIDAY	Design of Half and Full Adders, Half and Full Subtractors	CO2
4th	WEDNESDAY	Binary Parallel Adder, Multiplexer, Demultiplexers	CO2
	THURSDAY	Decoders, and Priority Encoder	CO2
	FRIDAY	SR- Flip flops	CO2
5th	WEDNESDAY	JK- Flip flops	CO2
	THURSDAY	T-Flip flops	CO2
	FRIDAY	D- Flip flops	CO2
6th	WEDNESDAY	Design of clocked sequential circuits	CO2
	THURSDAY	Design of Counters	CO2
	FRIDAY	Shift registers, Universal Shift Register.	CO2
7th	WEDNESDAY	Stable and Unstable states, output specifications	CO3
	THURSDAY	cycles and races, state reduction	CO3
	FRIDAY	race free assignments, Hazards, Essential Hazards	CO3
8th	WEDNESDAY	Pulse mode sequential circuits	CO3
	THURSDAY	Design of Hazard free circuits	CO3
	FRIDAY	Basic memory structure –ROM -PROM – EPROM – EEPROM –EAPROM	CO3
9th	WEDNESDAY	RAM – Static and dynamic, RAM – Programmable Logic Device	CO3
	THURSDAY	Programmable Logic Array (PLA) –Programmable Array Logic (PAL)	CO3

	FRIDAY	Field Programmable Gate Arrays (FPG	CO3
10th	WEDNESDAY	Hardware Architecture	CO4
	THURSDAY	Hardware Architecture	CO4
	FRIDAY	Pin diagram	CO4
11th	WEDNESDAY	Pin diagram	CO4
	THURSDAY	Functional Building Blocks of Processor	CO4
	FRIDAY	Functional Building Blocks of Processor	CO4
12th	WEDNESDAY	Memory organization	CO4
	THURSDAY	I/O ports and data transfer concepts	CO4
	FRIDAY	Timing Diagram – Interrupts.	CO4
13th	WEDNESDAY	Instruction – format and addressing modes	CO5
	THURSDAY	Assembly language format	CO5
	FRIDAY	Data transfer	CO5
14th	WEDNESDAY	Data manipulation & control instructions	CO5
	THURSDAY	Programming: Loop structure with counting & Indexing	CO5
	FRIDAY	Look up table	CO5
15th	WEDNESDAY	Subroutine instructions	CO5
	THURSDAY	stack -8255 architecture and operating modes	CO5
	FRIDAY	stack -8255 architecture and operating modes	CO5

22/06/26

Signature of Faculty Concerned
(Electrical Engg.)

22/6/2026

Head of Department
(Electrical Engg.)

H.O.D.
Electrical Engg
SIET, KORAPUT

22/06/2026

Principal
S.I.E.&T, KORAPUT

Principal
Siddharth Institute of Engineering &
Technology Ektaguda, Koraput